Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

ATTY DOCKET NO.	SERIAL NO.
240586US2	10/623,557
APPLICANT: Takashi IPPOSHI	
FILING DATE: July 22, 2003	GROUP: 2822

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	2002-134374	05/10/2002	JAPAN (corr. USSN 09/930,202)		X
	AP	7-335511	12/22/1995	JAPAN (with English extract)		X
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

AW	Y. HIRANO, et al., IEEE International SOI Conference, pages 131-132, "BULK-LAYOUT-COMPATIBLE 0.18μm SOI-CMOS TECHNOLOGY USING BODY-FIXED PARTIAL TRENCH ISOLATION (PTI)", October 1999
AX	S. MAEDA, et al., IEDM, pages 129-132, "SUPPRESSION OF DELAY TIME INSTABILITY ON FREQUENCY USING FIELD SHIELD ISOLATION TECHNOLOGY FOR DEEP SUB-MICRON SOI CIRCUITS", 1996
AY	L-J. HUANG, et al., Symposium on VLSI Technology Digest of Technical Papers, pages 57-58, "CARRIER MOBILITY ENHANCEMENT IN STRAINED Si-On-INSULATOR FABRICATED BY WAFER BONDING", 2001
AZ	

☐ Additional References sheet(s) attached

Examiner: [signature] Date Considered: 2/26/04

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.